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~~SIMULTANEOUS BIDIRECTIONAL PORT WITH~~ SYNCHRONIZATION

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~~SIMULTANEOUS BIDIRECTIONAL PORT WITH SYNCHRONIZATION~~

Field

The present invention relates generally to digital data ports, and more specifically to bidirectional digital data ports.

Background of the Invention

Integrated circuits typically communicate with other integrated circuits on wires that are part of a "bus." A typical bus includes many wires, or circuit board traces, connecting multiple integrated circuits. Some buses are "unidirectional," because signals only travel in one direction on each wire of the bus. Other buses are "bidirectional," because signals travel in more than one direction on each wire of the bus. In the past, most bidirectional buses were not "simultaneously bidirectional," because multiple signals did not travel on the same wire in opposite directions at the same time; instead, the bus was shared over time, and different signals traveled in different directions at different points in time. Some newer buses are "simultaneous bidirectional" buses. Simultaneous bidirectional buses allow data to travel in two directions on a single wire at the same time.

Before reliable communications can take place on a bus, the integrated circuits need to be ready to communicate, or be "synchonized," and each circuit on the bus should have information regarding the readiness of other circuits on the bus. Some circuits may need to be initialized, while others may need to become stabilized. In some bus applications, it can take an indeterminate amount of time for circuits to become ready to reliably communicate. It can be important to not drive data onto a bus until the intended receiver is ready to receive the data, especially in simultaneous bidirectional bus applications, where data is being driven in both directions at once.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the

present specification, there is a need in the art for a method and apparatus to provide a synchronization mechanism for simultaneous bidirectional data buses.

Brief Description of the Drawings

Figure 1 shows a system employing simultaneous bidirectional ports;

Figure 2 shows a diagram of two synchronization circuits coupled together;

Figure 3 shows a timing diagram of the operation of the circuit of Figure 2;

Figure 4 shows a simultaneous bidirectional port circuit with closed loop impedance control;

Figure 5 shows a driver with controllable output impedance;

Figure 6 shows a driver with controllable output slew rate; and

Figure 7 shows a simultaneous bidirectional port circuit with impedance and slew rate control.

Description of Embodiments

In the following detailed description of the embodiments, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. Moreover, it is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described in one embodiment may be included within other embodiments. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The method and apparatus of the present invention provide a mechanism to synchronize multiple simultaneous bidirectional ports on the same bus. A synchronization circuit having imbalanced output impedance is coupled to another synchronization circuit on a bidirectional bus. The imbalanced output impedance is generated by differently sized pullup transistor and pulldown transistors. In one embodiment, a PMOS pullup transistor has an output impedance approximately equal to ten times the output impedance of an NMOS pulldown transistor. A receiver with input hysteresis has an input node coupled to the output of the driver. The hysteresis is satisfied when drivers from both simultaneous bidirectional ports assert output signals, thereby alerting both ports that each is ready to communicate.

Figure 1 shows a system employing simultaneous bidirectional ports. System 100 includes integrated circuits 102 and 104 interconnected by conductors 130 and 140. Integrated circuit 102 includes processor 106, bidirectional port 108, initialization circuit 110, and synchronization circuit 112. Integrated circuit 104 includes processor 116, bidirectional port 118, initialization circuit 120, and synchronization circuit 122. In the embodiment shown in Figure 1, integrated circuits 102 and 104 are shown having substantially similar circuits, such as processors 106 and 116. In other embodiments, integrated circuits 102 and 104 do not have substantially similar circuits. For example, integrated circuits 102 and 104 can be processors, processor peripherals, memory devices including dynamic random access memories (DRAM), memory controllers, or any other integrated circuit employing simultaneous bidirectional ports.

Integrated circuits 102 and 104 are agents on a simultaneous bidirectional bus. The simultaneous bidirectional bus can include any number of signal lines, but for simplicity, Figure 1 shows one signal line, conductor 140. Likewise, agents on the simultaneous bidirectional bus can include any number of bidirectional ports, and bidirectional ports can include any number of drivers and receivers. To simplify the explanation, each of integrated circuits 102 and 104 are shown with a single bidirectional port.

Integrated circuits 102 and 104 communicate with each other using bidirectional ports 108 and 118. Each bidirectional port sends and receives data on conductor 140. Initialization circuits 110 and 120 operate to initialize all or portions of integrated circuits 102 and 104. For example, in some embodiments, initialization circuit 110 initializes a control loop in bidirectional port 108. Examples of control loops that can be initialized include variable output impedance circuits and variable slew rate circuits. Other types of initialization operations can be performed by initialization circuit 110 without departing from the scope of the present invention.

Integrated circuits 102 and 104 also communicate with each other using synchronization circuits 112 and 122. Each synchronization circuit communicates with the other using conductor 130. In operation, synchronization circuits 112 and 122 alert each other that initialization of the respective integrated circuit is complete. When initialization of both integrated circuits is complete, each synchronization circuit can report this to the integrated circuit within which it is situated. For example, when initialization circuit 120 reports to synchronization circuit 122 that initialization is complete, synchronization circuit 122 can assert a signal on conductor 130. When initialization circuit 110 within integrated circuit 102 completes initialization, synchronization circuit 112 can assert another signal on conductor 130. When both synchronization circuits 112 and 122 have asserted signals on conductor 130, initialization of both integrated circuits 102 and 104 is complete. At this time, synchronization circuits 112 and 122 can report to integrated circuits 102 and 104, respectively, that initialization on both ends of the simultaneous bidirectional bus is complete, and the agents on the bus are ready to communicate.

In some embodiments, initialization circuit 110 initializes bidirectional port 108, and alerts synchronization circuit 112 when initialization is complete. For example, a closed loop impedance control circuit can initialize the output impedance of a data driver in bidirectional port 108, and directly notify synchronization circuit 112 when the output impedance of the data driver is set. In other embodiments, initialization circuit 110 communicates with processor 106 to report the completed initialization, and processor 106 communicates with synchronization circuit 112.

In some embodiments, when synchronization circuits 112 and 122 both report that initialization is complete, synchronization circuit 112 within integrated circuit 102 notifies processor 106. This can be performed through an interrupt, by polling, or by any other suitable processor communication mechanism. Processor 106 then communicates with bidirectional port 108 to report that initialization is complete, and that simultaneous bidirectional communications can take place.

The initialization provided by initialization circuits 110 and 120 can be performed at system startup, or after an event that cause a re-initialization. For example, when system power is applied, initialization circuits 110 and 120 provide start-up initialization. Also for example, when a portion of system 100 is reset or is subject to a large noise event, re-initialization may take place. Initialization can also take place during a hot-swap event, when one or more system components are removed or added to the system while power is applied.

In the embodiment shown in Figure 1, initialization circuit 110 is shown separate from processor 106 and bidirectional port 108. This structure emphasizes the initialization of the bidirectional port. In other embodiments, the initialization function is performed by dedicated circuitry within the bidirectional port, and in other embodiments, the processor performs all or part of the initialization functions.

Figure 2 shows a diagram of two synchronization circuits coupled together. Synchronization circuit 112 is a synchronization circuit within one agent on a simultaneous bidirectional bus, and synchronization circuit 122 is a synchronization circuit within another agent on the same simultaneous bus. For the purposes of explanation, synchronization circuit 112 is considered to be within the "A" agent on the simultaneous bidirectional bus, and synchronization circuit 122 is considered to be within the "B" agent on the same simultaneous bidirectional bus. Nodes and signals pertaining to the synchronization circuit 112 are prefixed with the letter "A," and nodes and signals pertaining to synchronization circuit 122 are prefixed with the letter "B."

Synchronization circuit 112 includes receiver 212, and a driver that includes inverter 204, P-channel Metal Oxide Semiconductor (PMOS) transistor 206 and N-

channel Metal Oxide Semiconductor (NMOS) transistor 208. Synchronization circuit 112 has an internal interface and an external interface. The internal interface includes node 202 and 214. The signal on node 202 is termed the "AREADY" signal, and the signal on node 214 is termed the "ANEIGHBOR" signal. The external interface includes the output of the driver at node 210, labeled "ASYNC." Synchronization circuit 122 includes corresponding interfaces, nodes, and signals, prefixed with the letter "B."

The sizes of PMOS transistor 206 and NMOS transistor 208 are arranged such that the output impedance of PMOS transistor 206 is substantially larger than the output impedance of NMOS transistor 208, and such that the output impedance of NMOS transistor 208 substantially matches the impedance of conductor 130. In some embodiments, the output impedance of PMOS transistor 206 is set to be at least ten times that of NMOS transistor 208 and conductor 130. For example, in the embodiment shown in Figure 2, both conductor 130 and NMOS transistor 208 have an impedance of Z_0, and PMOS transistor 206 has an impedance of $10Z_0$.

In operation, when agent A is ready to communicate, such as when initialization is complete, the AREADY signal on node 202 of the internal interface is asserted high. AREADY can be asserted by a processor, such as processor 106, or by a dedicated circuit, such as initialization circuit 110 (Figure 1). Prior to the assertion of the AREADY signal, NMOS transistor 208 is on and PMOS transistor 206 is off. As long as the driver within synchronization circuit 122 is in the same state, then the ASYNC signal on node 210 is substantially at the reference potential connected to the source of NMOS transistor 208. When the AREADY signal is asserted, NMOS transistor 208 is turned off and PMOS transistor 206 is turned on. As a result, the ASYNC signal on node 210 increases in voltage. Because the output impedance of PMOS transistor 206 is much greater than the impedance of conductor 130, a voltage divider is formed that keeps the voltage of the ASYNC signal from rising very far. When both synchronization circuits assert signals onto conductor 130, then the voltage of both the ASYNC signal and the BSYNC signal will rise to close to the positive reference connected to the drain of PMOS transistor 206.

Receivers 212 and 232 have inputs with hysteresis, commonly referred to as "Schmitt triggers." The hysteresis of receivers 212 and 232 ensures that the output nodes change state only when the voltage on the input node satisfies the hysteresis. For example, the output of receiver 212 will change state when the voltage on the input node travels through the center point of the logic voltage swing plus a voltage delta. Likewise, the output node will change state in the other direction only when the input hysteresis is satisfied in the other direction. This provides noise immunity on the input to the receivers.

When one of AREADY or BREADY is asserted by the respective agent, the input nodes of receiver 212 and 232 will experience various voltage values as the signal reflects back and forth on conductor 130, but the input voltage value will not be high enough to satisfy the hysteresis of either receiver 212 or 232. Only when both AREADY and BREADY are asserted will the hysteresis in receivers 212 and 232 be satisfied, causing the ANEIGHBOR and BNEIGHBOR signals to be asserted. When the ANEIGHBOR signal is asserted, the agent that includes synchronization circuit 112 has an indication that both of the agents on the simultaneous bidirectional bus are ready to communicate, and when BNEIGHBOR is asserted, the agent that includes synchronization circuit 122 has an indication that both of the agents on the simultaneous bidirectional bus are ready to communicate.

Figure 3 shows a timing diagram of the operation of the circuit of Figure 2. The operation just described with respect to AREADY being asserted prior to BREADY being asserted is shown in Figure 2. AREADY is asserted high at 302. This corresponds to NMOS transistor 208 turning off and PMOS transistor 206 turning on. ASYNC is shown increasing in voltage at 308 as a result of AREADY being asserted at 302. After a time equivalent to the electrical length of the transmission line, BSYNC rises in voltage at 310. BSYNC does not rise as high as ASYNC because the termination at node 230 is substantially equal to the line impedance, Z_0. It should be noted that it is not necessary for the pulldown impedance of either driver to equal the line impedance, but that this condition provides a satisfactory termination. After a time equal to one round-trip electrical

length of the transmission line, ASYNC reduces in voltage as shown by 314. Prior to the assertion of BREADY, small reflections (not shown) travel back and forth on the transmission line (conductor 130).

Receiver threshold 306 is the voltage level necessary for either ASYNC or BSYNC to satisfy the hysteresis of either receiver 212 or 232. As can be seen in Figure 3, the initial voltage step launched into the transmission line falls short of threshold 306 by margin 312. Margin 312 is large in part because the pullup to pulldown impedance ratio of the drivers in synchronization circuits 112 and 122 is ten to one. Other impedance ratios can be used while still maintaining adequate margin 312 so that neither ANEIGHBOR nor BNEIGHBOR is falsely asserted.

When BREADY is asserted at 304, BSYNC increases in voltage correspondingly at 316. With both AREADY and BREADY asserted, both ASYNC and BSYNC eventually increase in voltage enough to surpass receiver threshold 306, causing ANEIGHBOR and BNEIGHBOR to assert within synchronization circuits 112 and 122, respectively. Because of the impedance mismatch between line 130 and PMOS transistors 206 and 226, reflections continue to bounce back and forth across line 130 until the voltage settles out close to Vcc. The reflections are shown at 320.

The relative impedance of the pullup and pulldown transistors and the transmission line, and the hysteresis of the Schmitt trigger receivers can be varied to vary margin 312 and the amount of time (or number of reflections) before ASYNC and BSYNC cross receiver threshold 306. For example, in the embodiment shown in Figure 2, the pullup to pulldown impedance ratio is ten to one and the ratio of the pulldown transistor to transmission line impedance ratio is one to one. In some embodiments, the pullup to pulldown ratio is five to one. This decreases margin 312, but also decreases the amount of time between the assertion of both AREADY and BREADY and when ASYNC and BSYNC cross the receiver threshold.

As can be seen from Figures 2 and 3, in some embodiments, the output impedance of the drivers is imbalanced with a pulldown impedance of substantially Z_0 and a pullup impedance of substantially $10Z_0$. As a result, the READY signal on

both agents must be asserted in order for the SYNC signals to rise high enough to satisfy the hysteresis of the receivers, thereby asserting the NEIGHBOR signals on each agent. Moreover, any glitch that occurs when only one end of the link asserts the READY signal is reduced because the pullup impedance is weak compared to the pulldown impedance and compared to the link impedance of Z_0. Also, setting the threshold of the Schmitt trigger receivers higher than the initial voltage step into the line prevents the NEIGHBOR signal from false assertions.

Figure 4 shows a simultaneous bidirectional port circuit with closed loop impedance control. Simultaneous bidirectional port circuit 400 is a bidirectional port circuit such as bidirectional port circuit 108 or 118 (Figure 1). Closed loop impedance control circuit 450 is an initialization circuit in an integrated circuit, such as initialization circuit 110 or 120. Simultaneous bidirectional port circuit 400 includes driver 402, receiver 404, multiplexer 410 and voltage references 406 and 408. The output node of driver 402 drives conductor 140, and is also the input node for receiver 404. Conductor 140 is simultaneously driven by another driver in another simultaneous bidirectional port circuit, and receiver 404 determines the logic value driven on conductor 140 by the other driver. For example, referring now back to Figure 1, bidirectional ports 108 and 118 both include drivers and receivers such as driver 402 and receiver 404. The receiver in bidirectional port 108 determines the logic value driven on conductor 140 by the driver in bidirectional port 118, and the receiver in bidirectional port 118 determines the logic value driven on the conductor by the driver in bidirectional port 108.

Referring again to Figure 4, receiver 404 compares the voltage value on conductor 140 to the voltage value of either reference 406 or reference 408 depending on the state of the outgoing data on node 412. The outgoing data steers multiplexer 410 so that one of reference 406 and reference 408 is present on one of the inputs to receiver 404. Details of one embodiment of a simultaneous bidirectional port can be found in U.S. Patent 5,604,450, issued Feb. 18, 1997.

Driver 402 is a driver having a controllable output impedance, one embodiment of which is shown in Figure 5. The output impedance of driver 402 is

controlled by closed loop impedance control circuit 450. Closed loop impedance control circuit 450 includes sample and compare circuit 454, up/down counter 452, dummy driver 458, and digital filter 460. The control loop is formed by sample and compare circuit 454, up/down counter 452, and dummy driver 458. Dummy driver 458 is terminated with resistor 464. In some embodiments, resistor 464 is a precision resistor external to the integrated circuit that includes closed loop impedance control circuit 450. This allows a system designer to select a value for resistor 464, thereby selecting a reference voltage present on node 466.

The voltage on node 466, which is a function of the output impedance of dummy driver 458, is compared with a target voltage on node 468 by sample and compare circuit 454. In some embodiments, sample and compare circuit 454 is an analog comparator that samples the voltage values on nodes 466 and 468, compares them, and produces a digital signal on the output to signify which of the two input voltage values is larger. The output of sample and compare circuit 454 controls the counting of up/down counter 452. Up/down counter 452 produces an unfiltered impedance control value on node 470, which controls the output impedance of dummy driver 458, and closes the loop. When the impedance of dummy driver 458 needs to be decreased, up/down counter 452 counts in one direction, and when the impedance of dummy driver 458 needs to increase, up/down counter 452 counts in the other direction. The unfiltered impedance control value on node 470 can include a single bit, but can also include a plurality of bits. When a single bit is used, the impedance value toggles between two values, and when N bits are used, the impedance can take on any of 2^N different values.

When the control loop of impedance control circuit 450 locks, the unfiltered impedance control signal alternates between two values. This results from the fact that the change in output impedance of dummy driver 458 causes the voltage on node 466 to surpass the voltage on node 468. In one embodiment, for each successive clock cycle thereafter, the unfiltered impedance control signal on node 466 alternates counting up and down as the voltage on node 466 alternates higher and lower than the target voltage on node 468.

Impedance control circuit 450 also includes digital filter 460. Digital filter 460 receives the unfiltered impedance control value on node 470 and produces a filtered impedance control value on node 472. The filtered impedance control value on node 472 controls the output impedance of driver 402 in simultaneous bidirectional port 400. When the loop is locked and the unfiltered impedance control signal alternates between two values, digital filter 460 provides a steady state filtered impedance control signal to driver 402 on node 472. In addition, when the loop is locked, the digital filter outputs a READY signal on node 462, signifying that the closed loop impedance control circuit has initialized. This corresponds to the AREADY signal on node 202 (Figure 2).

The closed loop impedance control circuit of Figure 4 is but one example of an initialization circuit that can be used in a system such as system 100 (Figure 1). In this example, the READY signal is generated directly from digital filter 460 in closed loop impedance control circuit 450. In other embodiments, closed loop impedance control circuit 450 communicates with a processor, such as processor 106 (Figure 1), and the processor relays the READY information to a synchronization circuit such as synchronization circuit 112 (Figure 1).

The closed loop impedance circuit of Figure 4 can initialize the output impedance of driver 402 during system initialization (e.g., at power-up), or can re-initialize the impedance of driver 402 after an event has changed the impedance. Example events include a noise spike in the system, or a hot-swap event. When a noise spike changes the voltage on resistor 464, the loop becomes unlocked, and the READY signal on node 462 is de-asserted while the loop re-locks (or "re-initializes"). A hot-swap event can occur when a system component is removed from a system while the power is on. During a hot-swap event, when a new system component is installed, the initialization takes place, and the READY signal is asserted when the initialization is complete.

Figure 5 shows a driver with controllable output impedance. Driver 500 is a driver, such as driver 402, capable of driving a bidirectional data line. The enable

signals (EN0-EN3) correspond to the impedance control value on node 472 (Figure 4).

Driver 500 includes input node 540 and output node 550. Input node 540 is coupled to the gate of PMOS transistor 520, and is also coupled to the gate of NMOS transistor 522. Taken together, PMOS transistor 520 and NMOS transistor 522 function as an inverter. Connected in a cascode arrangement with PMOS transistor 520 are parallel PMOS transistors 502, 504, 506, and 508. Likewise, connected in a cascode arrangement with NMOS transistor 522 are parallel NMOS transistors 512, 514, 516, and 518. Any number of parallel PMOS transistors and parallel NMOS transistors can be on at any time, thereby providing a variable output impedance at node 550. The parallel NMOS and PMOS transistors are sized with a binary weighting such that the output impedance can be controlled with a binary number. For example, PMOS transistor 502 and NMOS transistor 512 have an impedance value of "Z," PMOS transistor 504 and NMOS transistor 514 have an impedance value twice as great, and so on. The binary number in the embodiment of Figure 5 is four bits wide corresponding to the enable signals labeled EN0 through EN3.

The use of a binary weighted impedance control mechanism allows an up/down counter to be employed to modify the impedance one value at a time. As the control signals from the up/down counter count up, more (or larger) transistors are turned on, and the output impedance drops. Likewise, as the counter counts down, the output impedance increases.

In another embodiment, linear weighting is employed. Linear weighting allows a shift register or other similar component to control the output impedance by changing one bit at a time. A driver having linear weighted impedance control allows for precise control of the output impedance with reduced chance of glitches at the expense of increased signal lines and transistor count. For example, in the embodiment of Figure 5, four enable signals provide 16 different output impedance values. A linear weighted output driver with 16 impedance values includes 16 parallel NMOS transistors and 16 parallel PMOS transistors driven by 16 control

signals. Linear weighted drivers can be implemented without departing from the scope of the present invention.

Figure 6 shows a driver with controllable output slew rate. Driver circuit 600 includes a plurality of push-pull driver circuits 602_0 to 602_n. Each push-pull driver circuit includes a pullup transistor 604, a pullup resistor 606, a pulldown resistor 608, and a pulldown transistor 610. The series resistors of each push-pull driver circuit have a resistance which is relatively large in relation to an impedance of the transistors. As such, the series coupled resistors 606 and 608 dominate the series impedance, and the push-pull driver circuit has good linearity from power rail to power rail. The resistors can be fabricated from any suitable structure, such as an N-well layer of a standard CMOS process.

The number of push-pull driver circuits provided in driver circuit 600 is determined by a number of taps provided by a delay line circuit 620. That is, delay line circuit 620 includes a plurality of delay stages which are tapped to provide a number of delayed signals. In the embodiment illustrated in Figure 6, the delay line circuit has four taps. Each push-pull direr circuit is turned on in sequence, according to the delay between the taps in delay line 620. The output signal on node 612 transitions from ground to VCC in a plurality of discrete steps as the push-pull driver circuits turn on in sequence. The number of steps corresponds to the number (n+1) of push-pull driver circuits provided in the driver circuit. In some embodiments, the output signal on node 612 is filtered to provide a linearly varying signal as the push-pull driver circuits turn on or off.

Delay line 620 can be implemented in several ways. In one embodiment, the delay line can be implemented as a string of inverter circuits. This embodiment provides a resolution between consecutive tap output signals of two inverter delays. Two strings of inverters can be provided to achieve a resolution of one inverter, one driven by input data and the other driven by an inverse of the input data. In either embodiment, jitter may be experienced through the driver circuit that is close to jitter of a standard CMOS output circuit. To reduce this jitter, the delay line circuit can be coupled to receive a delay control signal from a delay locked loop circuit 624. The

delay of the delay circuit, therefore, is locked to a clock signal and remains stable with respect to process, voltage, and temperature variations. Further, low-to-high and high-to-low signal transitions in the tap output signals are equal.

In embodiments that include delay locked loop 624, a period of time lapses as the delay of the delay circuit is locked to the clock signal on node 626. When the delay locked loop is locked, delay locked loop 624 can produce a READY signal on node 628 to alert a synchronization circuit such as synchronization circuit 112 (Figure 2) that initialization is complete.

Driver circuit 600 is but one embodiment of a driver having output slew rate control. Other driver circuits can also be used. In addition, driver circuit 600 can be combined with driver circuit 500 (Figure 5) to create a single driver with variable output impedance and variable output slew rate.

Figure 7 shows a simultaneous bidirectional port circuit with impedance and slew rate control. Simultaneous bidirectional port circuit 700 is shown coupled to processor 720. In the embodiment illustrated in Figure 7, processor 720 controls the output impedance and slew rate of driver 702. When the output impedance and slew rate of driver 702 is initialized, processor 720 can assert the READY signal on node 722, thereby alerting a synchronization circuit that initialization is complete.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.